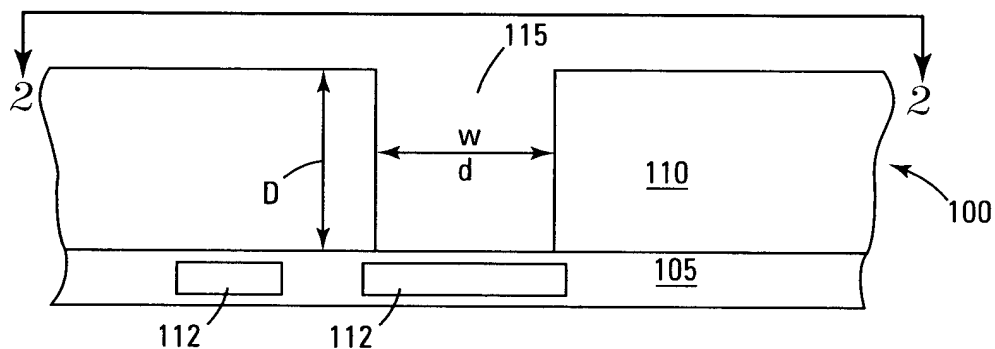
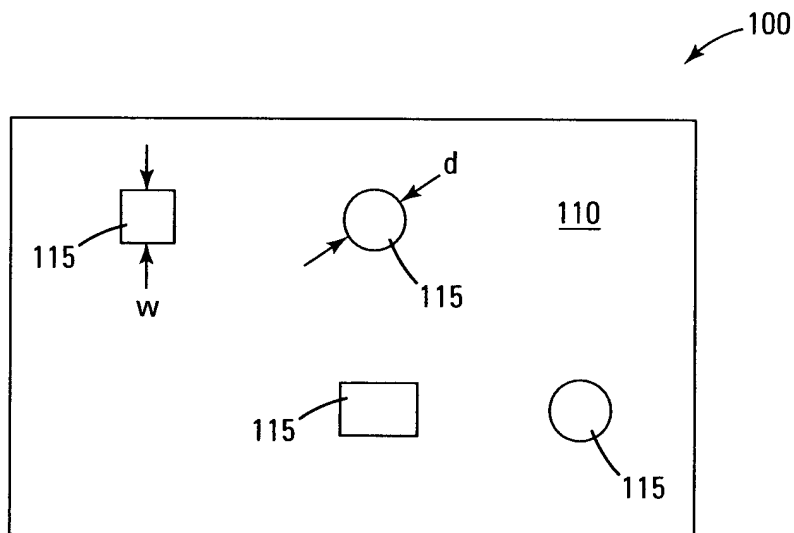




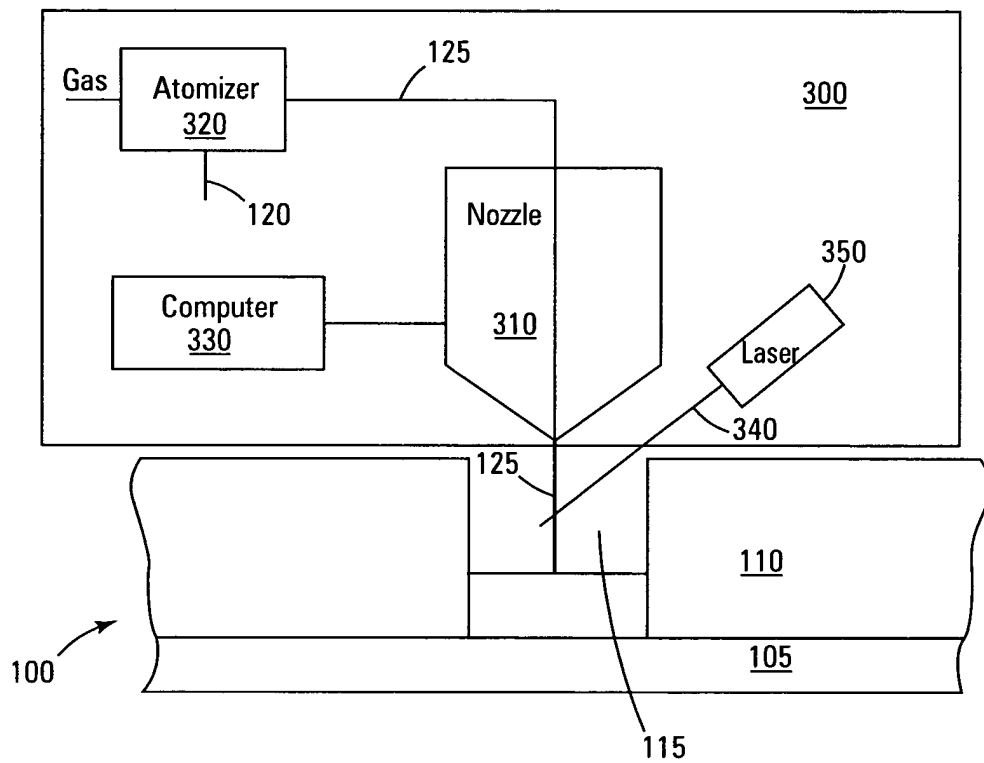
1/6



*Fig. 1*



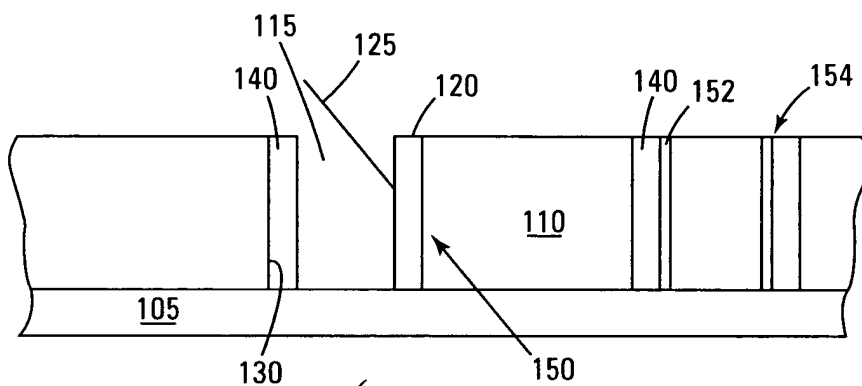
*Fig. 2*



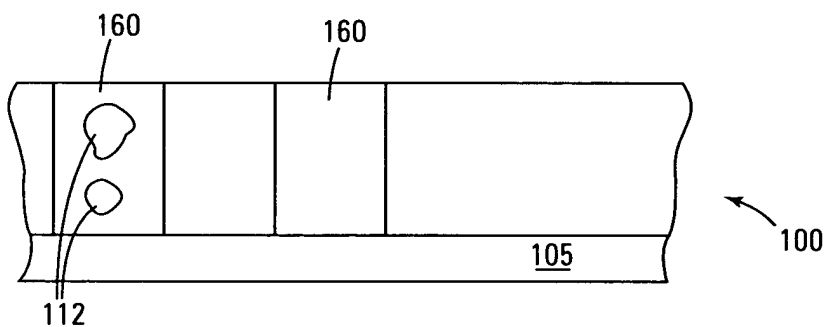
*Fig. 3*



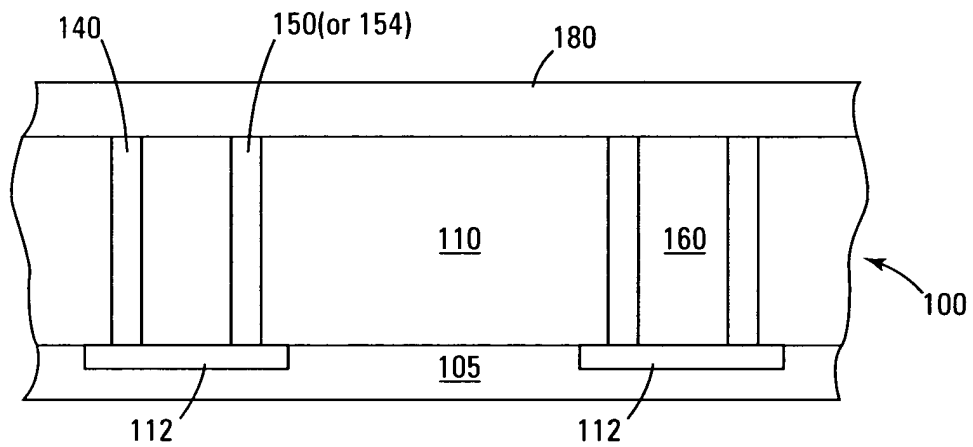
3/6



*Fig. 4*



*Fig. 5*



*Fig. 6*

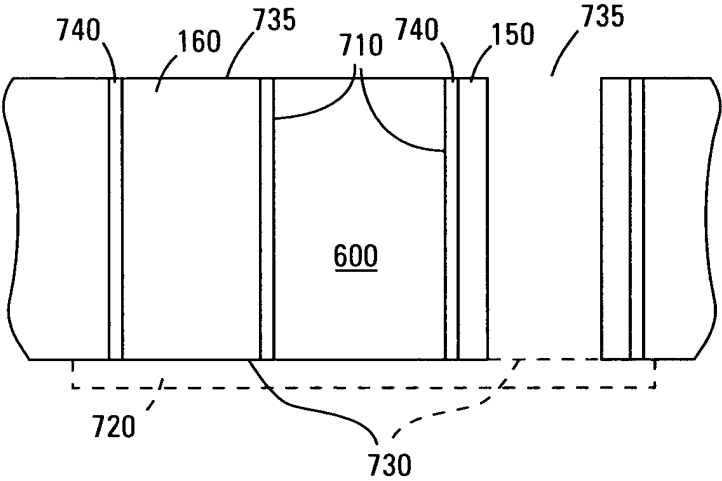


Fig. 7

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Diagram 800 illustrates a system architecture. A central array 842 is shown, which is a grid of elements. The array is divided into two main sections, 846a and 846b, by a vertical line 847b. The array is also divided into two main sections, 847a and 847b, by a horizontal line 846a. The array contains elements 843a, 843b, 843c, and 843d, which are arranged in a grid. The array is connected to an input 845 on the left, an output 844 on the top, and a control 848 on the bottom. The array is also connected to a control 848 on the bottom. The array is also connected to a control 848 on the bottom.

*Fig. 8*